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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/160,657	09/25/1998	JOSEPH W. LYDING	22010-135/IL	6611

24202 7590 10/09/2002

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EXAMINER	
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ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/09/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/160,657	LYDING ET AL.
	Examiner	Art Unit
	Jeff Vockrodt	2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 12 June 2002.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 40-48 and 60-81 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 40-48 and 60-81 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claims 40-48 & 60-81 are pending. A Final Office action was mailed on September 9, 2002 in which claims 79-81 were indicated allowable. In response, applicants filed an amendment under 35 U.S.C. § 116 on September 23, 2002 (Paper #36), which has not been entered. During a telephone conversation with N. Rhys Merritt on October 7, 2002 the examiner informed applicant that the allowability of claims 79-81 had been withdrawn in view of the newly cited reference to Okazaki et al., "Characteristics of Sub-1/4-μm Gate Surface Channel PMOSFET's Using a Multilayer Gate Structure of Boron-Doped Poly-Si on Thin Nitrogen-Doped Poly-Si," IEEE Transactions of Electron Devices, Vol. 41, No. 12, December 1994, pp. 2369-2375. ("Okazaki"). This office action is responsive to the amendment filed June 12, 2002.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 66-74 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 67-74 depend on claim 66, which requires "[a]n improved semiconductor transistor device having a gate and a film located adjacent said transistor gate and having a concentration of deuterium within said film, wherein the improvement comprises: <u>a concentration of at least about 10^{16} cm^{-3} of said deuterium being present in said film</u>, said transistor device susceptible to degradation associated with hot carrier

stress, said concentration of deuterium substantially reducing said degradation associated with said hot carrier stress." (emphasis added).

Applicants, to establish support for the subject matter of claims 66-74, allege that "the concentration of deuterium resulting from the disclosed annealing process is 'at least about 10^{16} cm^{-3}' is a result of the particular annealing process described in those applications and thus is inherently disclosed by each of those applications." paper no. 25, page 6. Applicants rely primarily on figure 4 of the Ference article which depicts SIMS deuterium profiles for anneals of different structures to support their theory of inherency. Figure 4 of Ference shows example B which is an <u>anneal in deuterium</u> under the conditions similar to those of the present application but occurring <u>at the first metal step</u>. This example of Ference results in a deuterium concentration at the gate oxide of greater than 10^{16} atoms/cc.

Application S.N. 08/586,411 fails to describe the process of example B in figure 4 of Ference with sufficient specificity to warrant a conclusion that the composition of deuterium in the gate oxide that is described by Ference is an inherent property of Applicants' written description. The portion of application S.N. 08/586,411 relied on is found at pages 10-11. "In this regard, deuterium conditioning or passivation of the device 12 can be achieved in a variety of ways. For instance, device 11 can be heated in the presence of a flowing, mixed, or static deuterium-enriched ambient at one or more stages of fabrication, and/or after fabrication is completed (i.e. after the metal contacts are completed)." Applicants must show that the claimed concentration <u>necessarily results</u> from what is described in application S.N. 08/586,411 and is not just a possible outcome that is achieved by picking and choosing certain processes from the disclosed list of process alternatives in the application. "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in

the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities and possibilities. The mere fact that a thing may result from a given set of circumstances is not sufficient" MPEP §2112 (quoting In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations omitted)). Applicants cannot meet the written description requirement for an allegedly inherent deuterium concentration by merely showing that the claimed deuterium concentration is achieved by post-fabrication annealing when the disclosure does not provide any direction leading one of ordinary skill in the art to choose post-fabrication annealing from annealing "at one or more stages of fabrication, and/or after fabrication is completed (i.e. after the metal contacts are completed)". Kropa v. Robie, 88 USPQ 478, 483 (CCPA 1951) (adequate disclosure for a count drawn to an abrasive article was not found where practicing the process disclosed in the application "would not inevitably or necessarily produce an abrasive article.").

In the request for reconsideration filed June 12, 2002, applicants assert that written-description support of the claimed subject matter is found at page 14-18 of the '411 application. The examiner finds that the example set forth therein only establishes a deuterium anneal that occurs at some point after the gate electrodes of the NMOS transistors are formed -- not post-metallization or after the metal contacts are formed. Applicants do not allege that an anneal after forming the gate electrode but before forming the contacts would inherently produce the claimed deuterium concentration in the device. The record suggests, on the other hand, that annealing before forming contacts is insufficient to produce any appreciable deuterium concentration. In remarks filed November 11, 2000, page 6, last paragraph, applicants state, "Clark et al have shown that, post fabrication, the deuterium at the silicon/ silicon dioxide interface due to

the earlier annealing process, will no longer effectively remain because of the higher temperature processing, subsequent to the deuterium annealing, required to form contacts to the MOSFET structures of Lisenker and Saks." Applicants' NMOS transistors disclosed in their example also require subsequent contact formation, which would effectively drive out, like in Lisenker, any deuterium that was added by the post-gate anneal in deuterium. Therefore, support for the deuterium concentration recited in claims 66-74 cannot be found in the written description, either expressly or under principles of inherency. Accordingly, claims 66-74 stand rejected under the written description requirement of 35 USC § 112.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 40-48, 60-65, and 75-78 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,514,628 ("Enomoto") in view of P.C.T. International Application WO 94/19829 ("Lisenker").

Lisenker teaches that where hydrogen is used to remove dangling bonds at the Si/SiO_2 interface in transistor gate oxides, page 2, ll. 10-25, substitution of hydrogen with deuterium results in transistors having improved stability, quality, and reliability, page 4, ll. 32-34. Lisenker, in discussing the many ways in which deuterium can be substituted for hydrogen, states that, "an annealing step is conducted in a deuterium atmosphere instead of a hydrogen atmosphere," pp. 5, ll. 5-15. Thus, Lisenker suggests improving

hydrogen anneal passivation steps, by substituting deuterium for hydrogen as an annealing gas in passivation processes.

Of the hydrogen annealing examples taught by Lisenker, there is no mention of a hydrogen annealing step occurring after electrical contacts are formed on a semiconductor device. Therefore, Lisenker alone does not teach a deuterium annealing step that occurs after electrical contacts have been formed over a semiconductor device.

Enomoto teaches a two step sinter (anneal) post metal hydrogen passivation method whereby a sufficient sinter operation is preceded by an insufficient sinter operation and a testing step. In discussing the background of the invention, Enomoto states that hydrogen anneal processes, "typically [occur] toward the end of the fabrication process," col. 1, ll. 59-62. In the preferred embodiment, the final and sufficient sinter step is carried out in a hydrogen atmosphere at a temperature of approximately 400°C for more than 30 minutes after forming electrical contacts, col. 3, ll. 30 & col. 4, ll. 25-35. The sufficient sinter step reduces interface traps by terminating dangling bonds with hydrogen.

Lisenker and Enomoto are analogous art. Both references teach reducing interface states in semiconductor devices to increase device reliability and performance by way of passivation.

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the hydrogen of the post metallization anneal step in Enomoto, with deuterium, as suggested by Lisenker. The motivation to combine references in this manner comes from Lisenker's teaching that deuterium is superior to hydrogen for increasing device quality and reliability, and that deuterium can be substituted for hydrogen in passivation processes.

In re claims 41, 60-61, and 63, the gate material is preferably silicon oxide.

In re claim 42 and 64, the silicon semiconductor layer is single crystal which is referred to in reference to the underlying crystal structure.

In re claim 43 and 75-78, Enomoto teaches that the sufficient sinter step (anneal) can last 30-60 minutes.

In re claim 44, Lisenker teach a silicon wafer (abstract) which in its ordinary usage implies a single crystal silicon wafer.

In re claims 45 and 75-78, Lisenker at page 1 incorporates by reference the article Sah, "Models and Experiments on Degradation of Oxidized Silicon", Solid-State Electronics, vol. 33, pp. 147-167. The Sah article at page 160 teaches a forming gas composition of 10% hydrogen and 90% nitrogen which is used for device passivation.

In re claim 46, figure 1 of Lisenker reference shows deuterium and hydrogen covalently bonded to silicon.

In re claim 47, the chip is subsequently packaged, Enomoto, col. 2, ll. 2-3.

In re claim 48 and 65, the existence of covalently bonded deuterium is suggested in the above combination, and shown by figure 1 of Lisenker.

In re claims 62-65 and 75-78, claim 62 Enomoto teaches a preferred temperature of 400°C, abstract.

Claims 40-48, 60-65, and 75-81 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okazaki et al., "Characteristics of Sub-1/4-µm Gate Surface Channel PMOSFET's Using a Multilayer Gate Structure of Boron-Doped Poly-Si on Thin Nitrogen-Doped Poly-Si," IEEE Transactions of Electron Devices, Vol. 41, No. 12, December 1994, pp. 2369-2375 ("Okazaki") in view of U.S. Pat. No. 5,864,161 ("Mitani") and P.C.T. International Application WO 94/19829 ("Lisenker").

Okazaki teaches a MOS transistor having a gate oxide of 3.5 nm (35 Angstroms) and 5 nm (50 Angstoms) (see e.g. Okazaki, page 2370, 1st full paragraph) that is

susceptible to hot carrier degradation (see e.g. Okazaki, page 2372, 2d col.). Okazaki acknowledges the trend of decreasing gate oxide thickness in deep submicrometer CMOS (see Okazaki, page 2369, "Introduction").

Mitani teaches a p-channel MOS transistor (Third Embodiment, col. 22) formed by a method comprising the steps of forming on a semiconductor substrate a gate oxide 203 (Fig. 21A) having a thickness of 10 nm (100 Angstroms) (col. 22, ll. 17-18); forming a gate stack, an oxide over the gate stack having contact holes, and contacts 214 (Fig. 21E); and performing an anneal in nitrogen containing 10% hydrogen at 450°C for 15 minutes, thereby completing an MOS transistor. Mitani establishes that post-contact anneals in hydrogen were well known and desirable for MOS transistors useful for CMOS applications.

Lisenker, as discussed previously in relation to claims 40-48, 60-65, and 75-78, teaches substituting deuterium for hydrogen in processes such as hydrogen anneals to reduce device degradation due to hot carrier stress.

Okazaki, Mitani, and Lisenker are analogous art because they are within the field of CMOS devices and relate to the problem of hot-carrier reliability.

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the post-contact anneal of Mitani modified to include deuterium in the transistor of Okazaki having a gate oxide of less than 55 angstroms. One of ordinary skill in the art would have been motivated to make these modifications by the expectation of improved hot carrier reliability as taught by Lisenker.

Claims 40-48, 60-65, and 75-81 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saks et al., "The Time-Dependence of Post-Irradiation Interface Trap Build-up in Deuterium Annealed Oxides," IEEE Transactions on Nuclear Science, Vol. 39, No. 6, December 1992, pp. 2220-2229 ("Saks") in view of Okazaki.

Saks teaches that transistors annealed in deuterium (D_2) exhibit 3.2 to 4.5 fold retardation factor relative to transistors annealed in hydrogen (H_2) (Saks, Table 1, page 2224). Saks teaches two annealing steps. First, Saks treats N-channel MOSFETS having a gate oxide thickness of 32.5 nm (325 Angstroms) by annealing in 100% deuterium (or hydrogen) after definition of the polysilicon gates and N+ source/drain region. This was the last high temperature (>500°C) step before measuring the lifetime characteristics to avoid out-diffusion (Saks, Sample Fabrication, page 2221). Second, Saks performs a post-contact "sinter" anneal at 400°C in 100% D_2 for 30 minutes (Saks, second column, page 2222). Saks teaches that these anneals are often carried out to reduce the initial interface trap density to improve operating characteristics and that they have no discernable effect on the radiation sensitivity of any of the three oxide types (Saks, second column, page 2222).

Saks differs from the claimed device by not teaching a gate oxide thickness within the claimed range. Saks teaches a 325 Angstrom gate oxide thickness while the claims require "a gate insulating film not exceeding about 55 angstroms."

Okazaki teaches a MOS transistor having a gate oxide of 3.5 nm (35 Angstroms) and 5 nm (50 Angstoms) (see e.g. Okazaki, page 2370, 1st full paragraph) that is susceptible to hot carrier degradation (see e.g. Okazaki, page 2372, 2d col.). Okazaki acknowledges the trend of decreasing gate oxide thickness in deep submicrometer CMOS (see Okazaki, page 2369, "Introduction").

Saks and Okazaki are analogous art because they are within the field of CMOS devices and relate to the problem of hot-carrier reliability.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a gate oxide thickness not exceeding 55 angstroms in the process of Saks. One of ordinary skill in the art would have been motivated to make this

manipulation by the trend for decreasing gate oxide thickness in CMOS and the fact that gate oxides within the claimed range had been produced at the time of the invention.

It is noted that the claims do not preclude both pre- and post- contact annealing. Additionally, there would appear to be no structural difference between a device that is subject to both a pre-anneal and a post-anneal in deuterium relative to a device subject to only a post-anneal in deuterium. Cf. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

Rejection of Claim Corresponding to Proposed Count

Claims 66-74 of this application have been copied by the applicants from U. S. Patent No. 6,023,093. These claim are not patentable to the applicants because they lack adequate written description under 35 USC § 112 1st paragraph for the claimed subject matter as set forth above.

An interference cannot be initiated since a prerequisite for interference under 37 CFR 1.606 is that at least one claim subject to a judgment in the interference be patentable to the applicants

Response to Arguments

Applicants' arguments filed June 12, 2002 have been fully considered but they are not persuasive.

Whereas applicants' arguments traversing the rejection under the written description requirement of 35 U.S.C. § 112 are noted, a response to these arguments is set forth above under the heading "Claim Rejections - 35 USC § 112."

With regard to the arguments traversing the rejection of claims 40-48, 60-65, and 75-78 under 35 U.S.C. 103(a) as being unpatentable over Lisenker in view of Enomoto, the examiner finds them unpersuasive.

First, Applicants argue that the problems addressed by Lisenker and Enomoto are distinct. Applicants state that Lisenker's concerns address annealing during device

processing to reduce device degradation due to hot carrier stress during operation and Enomoto is not directed to solving these problems. The examiner disagrees because the problem of "high sensitivity to hot carrier degradation" is but one effect of poor oxide quality that can be mitigated against by annealing in deuterium instead of hydrogen as recognized by Lisenker. (Lisenker, page 1). Enomoto is explicitly directed to improving the Si-SiO_2 interface by annealing in hydrogen. (Enomoto, e.g. col. 4, ll. 3-24).

Second, Applicants argue that the lifetime improvement characteristics recited in the final clause of claim 40 constitutes a measurable, structural characteristic of the device that is not found in the applied references. The Examiner does not agree. The lifetime improvement characteristics recited in the claim represent a functional aspect of the device. Whether a structure is imposed on the device by this functional limitation is unclear from the record. For instance, no data on this record suggest that the function is a result of the device structure that is distinct from Enomoto. In contrast, the specification seems to suggest that the lifetime improvement characteristic is generally brought about by using deuterium instead of hydrogen in transistor devices (specification, page 22, 2d paragraph).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning communications from the examiner should be directed to Jeff Vockrodt at (703) 306-9144 who can be reached on weekdays from 9:30 am to 5:00 pm EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian, can be reached at (703) 308-4905.

The fax numbers for this Group are (703) 305-3432, (703) 308-7722, (703) 305-3431, and (703) 308-7724. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist at (703) 308-0956.

October 7, 2002
J. Vockrodt

AMIR ZARABIAN
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